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PHOSPHOROUS-DOPED SILICON DIOXIDE PROCESS TO CUSTOMIZE CONTACT ETCH PROFILES

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BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0001] The present invention relates generally to processes for depositing doped silicon dioxide in the manufacture of integrated circuit devices. In particular, a method for depositing doped silicon dioxide is provided that improves the etch profile of contact holes etched into the silicon dioxide layer.

DESCRIPTION OF RELATED ART

[0002] In semiconductor devices, doped silicon dioxide is used to form insulating layers that electrically separate conduction layers from other conduction layers or transistor layers. The conduction layers are electrically connected through the insulating layer by metal filled holes, known as contacts or vias.

[0003] When forming the insulating layer, doped silicon dioxide is typically deposited using high density plasma chemical vapor deposition (HDPCVD). Contact holes are etched into the doped silicon dioxide layer with an etchant such as C_4F_8. A conductive metal such as tungsten is then deposited in the contact holes by chemical vapor deposition or other deposition technique.

[0004] The contact holes through the insulating layer must exhibit certain characteristics so that the metal deposited into the contact holes forms a good electrical connection. In particular, the etch profile of the contact holes must be controlled so that the deposited metal fills the holes and makes good contact to the underlying layer.

[0005] Figure 1 A is a cross-section of a device layer 105 that exhibit an undesirable etch

rofile known as "footing." Footing occurs when the doped silicon dioxide that is in the lower portion 107 of layer 105 is etched at a faster rate than the doped silicon dioxide that is in the upper portion 109 of layer 105.

[0006] Footing can cause, among other problems, poor contact between the metal used to fill the contact hole and the conductive layer beneath. For example, as illustrated by contact hole 201 of Figure 1A, the faster etch rate of the lower portion 107 of doped silicon dioxide layer 105 may create a contact hole 210 with a narrow neck 204. When, as illustrated in Figure 1B, a metal 212 is put into contact hole 201, the metal 212 may not completely fill hole 201, leaving the regions 214 unfilled. Metal 212 may not make contact, or may make only very poor contact, to the conduction layer 215.

[0007] Contact hole 220 of Figure 2 illustrates another potential etch profile problem that may result in poor contact to the conduction layer 215. The etch of hole 220 progressed horizontally instead of vertically, resulting in an incomplete etch of layer 105. The remaining material 222 of layer 105 prevents a metal from contacting the conductive layer 215 through the hole 220.

[0008] The problem of footing is becoming more significant as integrated circuit devices are made smaller and device features are more densely packed. In addition to the above described problems of poor contact, footing widens the contact hole and makes the exact dimensions of the contact hole difficult to control. As device dimensions shrink, the dimension tolerances also shrink, and thus the ability to control the etch profile of contact holes in doped silicon dioxide becomes more important.

SUMMARY

[0009] A method for depositing a doped silicon dioxide layer is provided that limits footing in contact holes etched into the layer so deposited. The method allows the dopant concentration in the silicon dioxide layer to be controlled throughout the layer so that the etch profile of contact holes subsequently etched into the layer can be controlled.

[0010] Dopant precursor gas and silicon-containing precursor gas are introduced into a plasma at an initial ratio of dopant precursor gas to silicon-containing gas. During an initial period of the deposition, while the temperature of the wafer is increasing, the initial ratio is changed to a final ratio, usually by increasing the ratio. During the final period of the deposition, while the wafer is at an essentially constant temperature, the ratio is held constant. The

concentration of dopant incorporated into the layer during the initial period is thus about the same as the concentration of dopant incorporated into the layer during the final period.

BRIEF DESCRIPTION OF THE FIGURES

[0011] Figure 1A (prior art) is a cross-sectional view of a contact hole in an insulating layer that has a footing etch profile with a narrow neck.

[0012] Figure 1B (prior art) illustrates the contact hole of Figure 1A filled with a metal.

[0013] Figure 2 (prior art) is a cross-sectional view of a contact hole in an insulating layer with a contact hole that has not been etched all the way through the insulating layer due to footing.

[0014] Figure 3 is a graph of the percentage of phosphorous dopant incorporated into silicon dioxide as a function of wafer temperature during deposition of the doped silicon dioxide.

[0015] Figure 4 is a graph of the change in wafer temperature during a typical doped silicon dioxide deposition and the corresponding graph of the amount of dopant incorporated into the layer.

[0016] Figure 5 is a block diagram illustrating a method of depositing a doped silicon dioxide layer so that contact holes etched into the layer have straight sidewalls and do not exhibit footing.

[0017] Figure 6 is a cross-sectional view of a contact hole having an etch profile that is too narrow in the lower portion.

[0018] Figure 7 is a graph illustrating of the amount of dopant incorporated into a silicon dioxide layer as a function of the amount of dopant precursor gas supplied during the deposition at three different temperatures.

DETAILED DESCRIPTION

[0019] It has been observed that the etch rate of a doped silicon dioxide layer is sensitive to the concentration of dopant in the layer, and that footing may be the result of non-uniform dopant concentration through the layer. The etch rate of phosphorous-doped silicon dioxide is faster in regions that have a higher concentration of dopant. Using conventional deposition methods, the lower portion of a doped silicon dioxide layer which is close to the substrate

surface, e.g., portion 107 of Figure 1A, typically has a higher dopant concentration than the upper portion of the layer (portion 109 of Figure 1A, which is often referred to as the bulk layer). Thus, lower portion 107 is etched faster, resulting in the footing problem described above in the text accompanying Figures 1A, 1B, and 2.

[0020] The cause of the variation in dopant concentration is related to the temperature of the wafer during the deposition process. Figure 3 is a graph 300 illustrating the concentration of phosphorous dopant in silicon dioxide (wt % P_2O_5) as a function of wafer temperature. Each point 302 in graph 300 corresponds to the phosphorous concentration in a silicon dioxide layer that was deposited at a particular temperature. The ratio of the flow rate of phosphine gas to the flow rate of silane gas was 1:2 (33% phosphine) for each deposition. It is clear from Figure 3 that at higher wafer temperatures the concentration of phosphorous dopant incorporated into silicon dioxide is reduced.

[0021] In conventional deposition processes, the wafer temperature is not constant throughout the deposition. Graph 400 of Figure 4 illustrates a change in wafer temperature during an exemplary deposition of a doped silicon dioxide layer. The wafer is typically preheated to, for example, 350° C before beginning the deposition. During an initial period 407 of the deposition, the wafer temperature increases until it reaches a final deposition temperature 408, which in this case is about 650°C.

[0022] As illustrated by graph 410 of Figure 4, which shows the dopant concentration as a function of depth of the deposited silicon dioxide layer, the change in wafer temperaturc shown in graph 400 affects the amount of dopant that is incorporated into the layer during deposition. The dopant concentration is higher in the lower portion 107 of the wafer, which is the portion deposited during the initial period 407 of the deposition, while the wafer is at a lower temperature. The dopant concentration levels off in the upper portion or bulk 109 of the layer, which is deposited while the wafer is at the relatively constant final temperature 408. Thus, the temperature changes during the deposition cause the amount of dopant that is incorporated into the silicon dioxide to be non-uniform throughout the layer.

[0023] To prevent footing, the silicon dioxide layer should have an essentially uniform dopant concentration throughout. A method for depositing a doped silicon dioxide layer with a more uniform dopant concentration throughout the layer is illustrated in Figure 5. In this method, the amount of dopant precursor gas supplied during the initial period 407 of the deposition is modulated to compensate for the higher amount of dopant that is incorporated into

the silicon dioxide layer while the wafer temperature is below the final deposition temperature 408.

[0024] As indicated in block 501 of Figure 5, the wafer is first transferred into the deposition chamber, typically an HDPCVD chamber, for example, the Speed™ reactor of Novellus Systems, Inc. (San Jose, CA). As indicated in block 502, the wafer is preheated, usually between 0 and 60 seconds, before the deposition is begun. The preheat is usually performed under idle plasma conditions, e.g., with He/O_2 or Ar/O_2 gases at the appropriate RF power, e.g., 3000 to 5000 W of low frequency power for 200 mm wafers. The preheat conditions may change for different size wafers.

[0025] The deposition is started, block 503, by introduction of precursor gases into the reaction chamber. The precursor gases include a silicon-containing precursor gas, for example silane or TEOS and a dopant precursor gas, for example phosphine (PH_3) or SiF_4. As indicated in block 503, the amount of dopant precursor gas introduced into the chamber at the beginning of the deposition, given as a ratio of the flow rate of the dopant precursor gas to the flow rate of the silicon-containing precursor gas (hereinafter "dopant/silicon ratio") is at an initial value. The initial value of the dopant/silicon ratio is typically lower than the final value (block 506) as described below.

[0026] As illustrated above in Figure 4, as the temperature of the wafer increases during the initial period 407 of the deposition, the amount of dopant incorporated into the silicon dioxide layer is reduced. To compensate for this reduction, the amount of dopant precursor gas introduced into the reaction chamber is increased during initial period 407. As shown in blocks 504 and 505, the amount of dopant precursor gas introduced into the chamber is increased in a series of *N* increments until the dopant/silicon ratio reaches the final value. The final value is the ratio that provides the desired dopant concentration in the bulk layer 109 at the final temperature. As shown in block 506, once the final value of the dopant/silicon ratio is reached, the deposition continues until the desired layer thickness is reached.

[0027] The amount of dopant precursor gas introduced into the chamber, both initially (block 503) and in each of the *N* increments (blocks 504/505), is adjusted so that the amount of dopant incorporated into the lower portion 107 of the silicon dioxide layer is the same as that incorporated into the bulk layer 109. The dopant/silicon ratio can be increased to its final value in a series of discrete increases, or by constantly increasing the dopant/silicon ratio until the final value is reached. Either method provides a relatively uniform dopant concentration throughout

the layer. As discussed above, the etch profile is very sensitive to the dopant concentration. The number of increments used to increase the dopant/silicon ratio should be sufficient so that the dopant concentration is sufficiently uniform to ensure the desired etch profile, e.g., an etch profile with straight sidewalls.

[0028] It is also important not to overcompensate for the increased incorporation of dopant during initial period 407 by using too low a ratio of dopant precursor gas to silicon precursor gas during initial period 407. Figure 6 illustrates a contact hole 600 having an etch profile that is obtained if too little dopant is incorporated into the silicon dioxide in lower portion 107. The etch profile will be too narrow at the bottom 612 of the contact hole 600, which may hinder good contact between a metal fill and the conduction layer 215.

[0029] The ratio of dopant precursor gas to silicon precursor gas to use during period 407 for a particular set of process conditions, dopant, and desired dopant concentration may be determined by trial and error, by performing a number of test depositions and etches until the desired etch profile is obtained. Alternatively, dopant profiles, such as those illustrated in graph 700 of Figure 7, can be measured for a series of test depositions at different temperatures and used to estimate the percentage of dopant precursor gas that will provide the desired dopant concentration. In the dopant profiles in graph 700, the wafer is held at a particular temperature, e.g., 400°C, 500°C, and 600°C, and the amount of dopant precursor gas is varied for each test deposition. The conditions of the test depositions, including He/O_2 or Ar/O_2 flow rate, RF powers, and chamber pressure are otherwise the same as will be used for the deposition to be performed by the method outlined in Figure 5. The concentration of dopant incorporated into a silicon dioxide layer at each ratio of dopant precursor gas is measured. In this way, the amount of dopant precursor gas that results in the desired concentration of dopant in the layer is determined for the particular temperature and set of process conditions being used.

[0030] The dopant profile information can be used with temperature profile information, such as that illustrated in graph 400 of Figure 4 and measured in a separate test deposition, to estimate the amount of dopant precursor gas to use initially and for each increment of initial period 407. The number *N* of increments and the length of each increment to use during initial period 407 of a deposition can also be estimated from the wafer temperature information. For example, for very large temperature differences between the initial and final deposition phases, more increments can be used. Longer increments or continuous dopant/silicon ratio adjustment can be used when the temperature change occurs more gradually.

[0031] After the deposition, the wafer is removed from the deposition chamber. To form the contact or via holes, the layer is typically planarized and a patterned mask is formed on the surface for the subsequent etch step, both by methods understood by those of skill in the art. The contact or via holes are then etched, typically by a dry etch method using C_4F_8, or by other methods also known to those of skill in the art. The resulting contact holes have straight sidewalls and do not exhibit footing.

[0032] The method illustrated in Figure 5 may be used for any dopant to improve the etch profile and reduce footing effects, for example, phosphorous by using PH_3 as the dopant precursor, fluorine by using SiF_4 as the dopant precursor, boron by using B_2H_6 as the dopant precursor, or boron in conjunction with phosphorous.

EXAMPLE

[0033] In an exemplary embodiment, contact holes etched into a phosphorous-doped silicon dioxide (PSG) layer formed by the method of Figure 5 have a good etch profile with straight sidewalls and without footing, as illustrated in Figure 8. In this example, two mass flow controllers control the SiH_4 flowrate, the PH_3 flowrate, and the dopant/silicon ratio. One mass flow controller is connected to a 100% SiH_4 source and the other mass flow controller is connected to a 50% SiH_4/50% PH_3 source. Specific conditions used to form the PSG layer are listed in Table 1:

Table 1	
PREHEAT	
LF power at 450 kHz	4000 W
O_2 flow rate	120 sccm
He flow rate	200 sccm
Time	30 seconds
Wafer temperature	to 350°C
DEPOSITION	
LF power at 450 kHz	4000 W
HF power at 13.56 MHz	2000 W
O_2 flow rate	500 sccm
He flow rate	100 sccm
SiH_4 flow rate	127.5 sccm for 2 seconds 122.5 sccm for 2 seconds 117.5 sccm for 2 seconds 112.5 sccm for 2 seconds 107.5 sccm for 106 seconds
PH_3 flow rate:	62.5 sccm for 2 seconds 67.5 sccm for 2 seconds 72.5 sccm for 2 seconds

	77.5 sccm for 2 seconds 82.5 sccm for 106 seconds

[0034] The total time for the deposition was 114 seconds, which produces a layer that is about 9000 Å thick. An HDPCVD reactor, the Speed™ reactor by Novellus Systems, San Jose, CA, was used for the deposition and the chamber pressure was maintained at a pressure of less than 10 mtorr. The final phosphine flow rate, 82.5 sccm (a ratio of phosphine to silane of 0.767:1), provided a dopant (P_2O_5) concentration in the top portion (bulk) of the layer of 9% by weight under constant temperature condition, i.e., when the final temperature (approximately 650°C) was reached. Each of the phosphine flow increments, 62.5, 67.5, 72.5, and 77.5 sccm, (providing ratios of 0.490, 0.551, 0.617, and 0.689, respectively) would provide 7.0%, 7.5%, 8.0%, and 8.5%, respectively, dopant concentration by weight in the top part (bulk) of the layer under constant temperature condition at the final temperature. However, because the temperature is low during the initial phase of the deposition, these lower flow rates provide closer to 9% dopant in the layer. Thus, a silicon dioxide layer having a relatively uniform dopant concentration of 9% by weight is produced.

[0035] During experimentation, when a flow rate that provides 6% dopant concentration in the bulk layer under steady state conditions was used for the initial percentage, the etch profile of the layer was narrower at the bottom, similar to the etch profile illustrated in Figure 6.

[0036] The embodiments of this invention described above are illustrative and not limiting. Many additional embodiments will be apparent to persons skilled in the art from the descriptions herein. For example, different deposition processes may have different temperature profiles, e.g., the temperature of the wafer may decrease at the end of the deposition. Using the methods described herein, the variation of dopant concentration within a layer due to any such temperature variations may be compensated for by adjusting the dopant precursor gas flow rates, to provide the desired etch profile. Similarly, using the methods described herein, a non-uniform doped silicon dioxide layer may be purposely deposited if it is desired to create a contact hole having a profile with a particular shape. These and other embodiments are intended to fall within the scope of the appended claims.